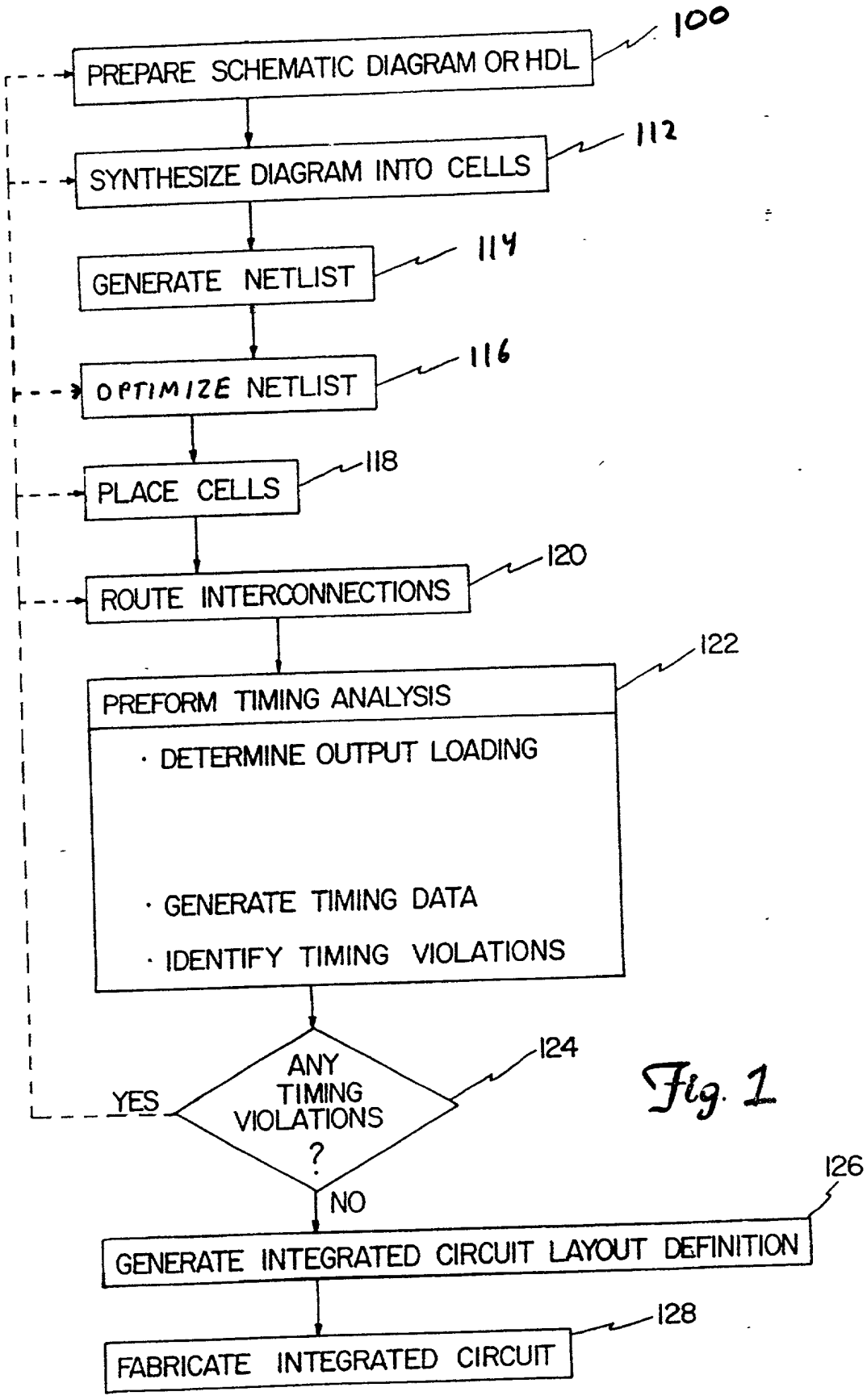
PREPARE SCHEMATIC DIAGRAM OR HDL
100
SYNTHESIZE DIAGRAM INTO CELLS
112
GENERATE NETLIST
114
OPTIMIZE NETLIST
116
PLACE CELLS
118
ROUTE INTERCONNECTIONS
120
PREFORM TIMING ANALYSIS
122
· DETERMINE OUTPUT LOADING
· GENERATE TIMING DATA
· IDENTIFY TIMING VIOLATIONS
ANY TIMING VIOLATIONS ?
124
YES
NO
GENERATE INTEGRATED CIRCUIT LAYOUT DEFINITION
126
FABRICATE INTEGRATED CIRCUIT
128

Fig. 1

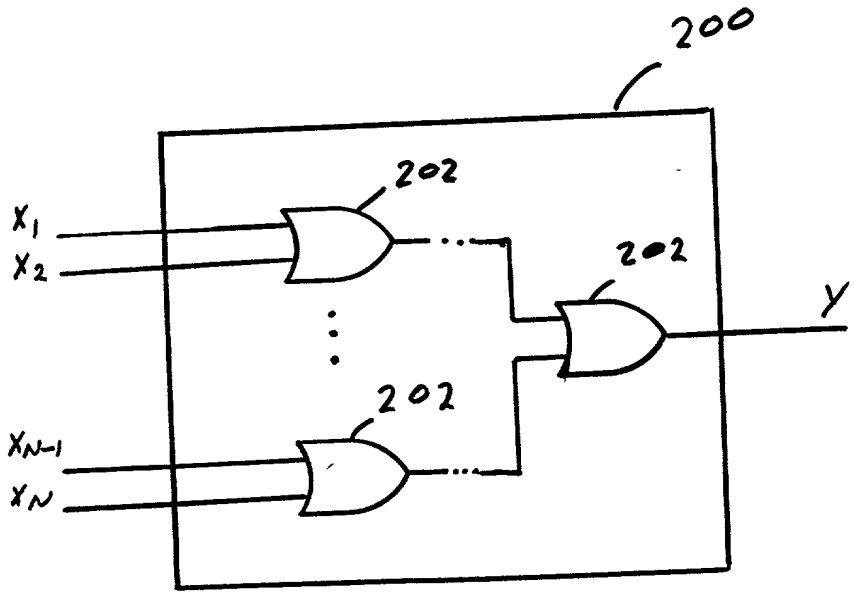
200
202
202
202
X_1
X_2
X_{N-1}
X_N
Y

FIG. 2

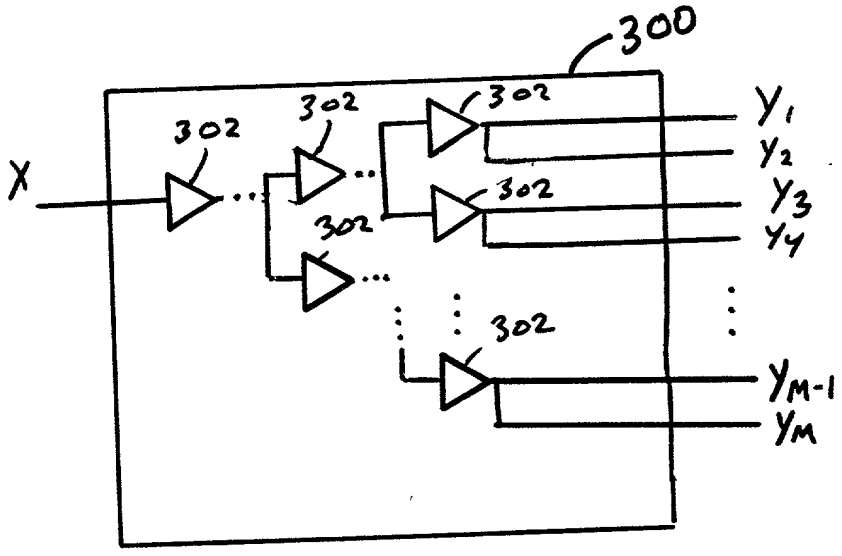
300
302
302
302
302
302
X
Y_1
Y_2
Y_3
Y_4
Y_{M-1}
Y_M

FIG. 3

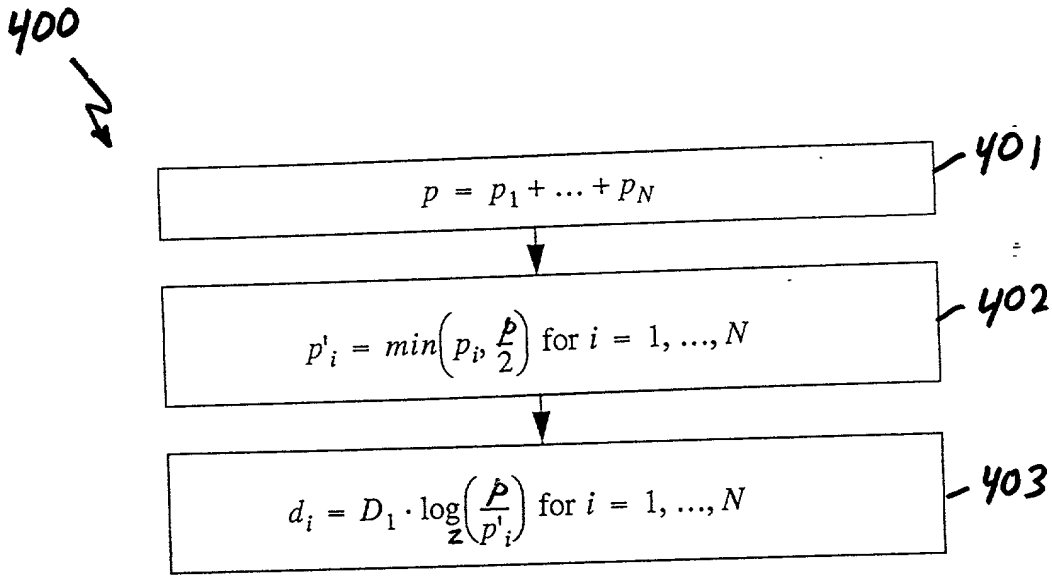
400
$p = p_1 + \ldots + p_N$
401
$p'_i = min\left(p_i, \frac{p}{2}\right)$ for $i = 1, \ldots, N$
402
$d_i = D_1 \cdot \log_z\left(\frac{p}{p'_i}\right)$ for $i = 1, \ldots, N$
403

FIG. 4

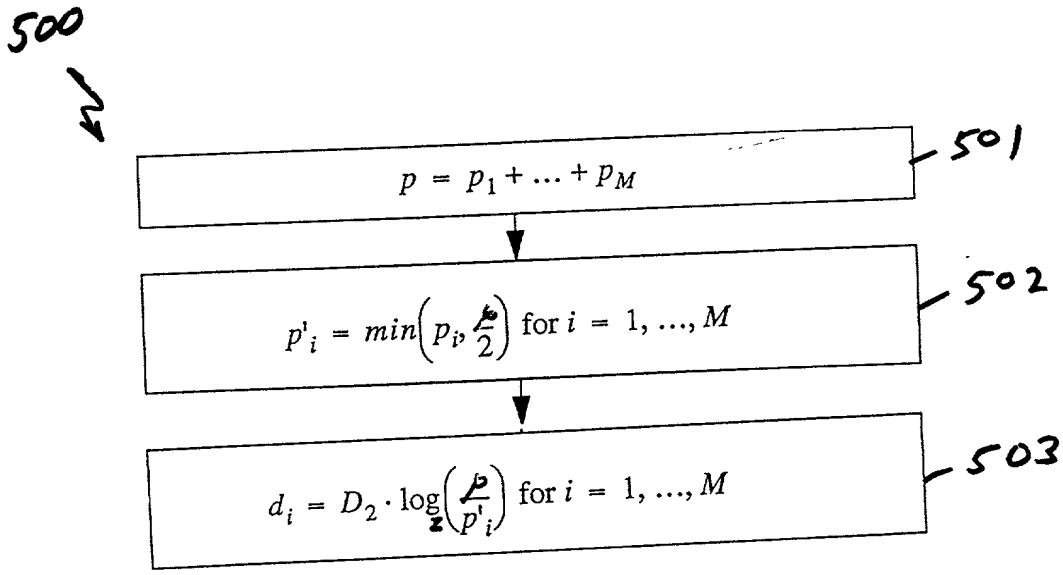
500
$p = p_1 + \ldots + p_M$
501
$p'_i = min\left(p_i, \frac{p}{2}\right)$ for $i = 1, \ldots, M$
502
$d_i = D_2 \cdot \log_z\left(\frac{p}{p'_i}\right)$ for $i = 1, \ldots, M$
503

FIG. 5

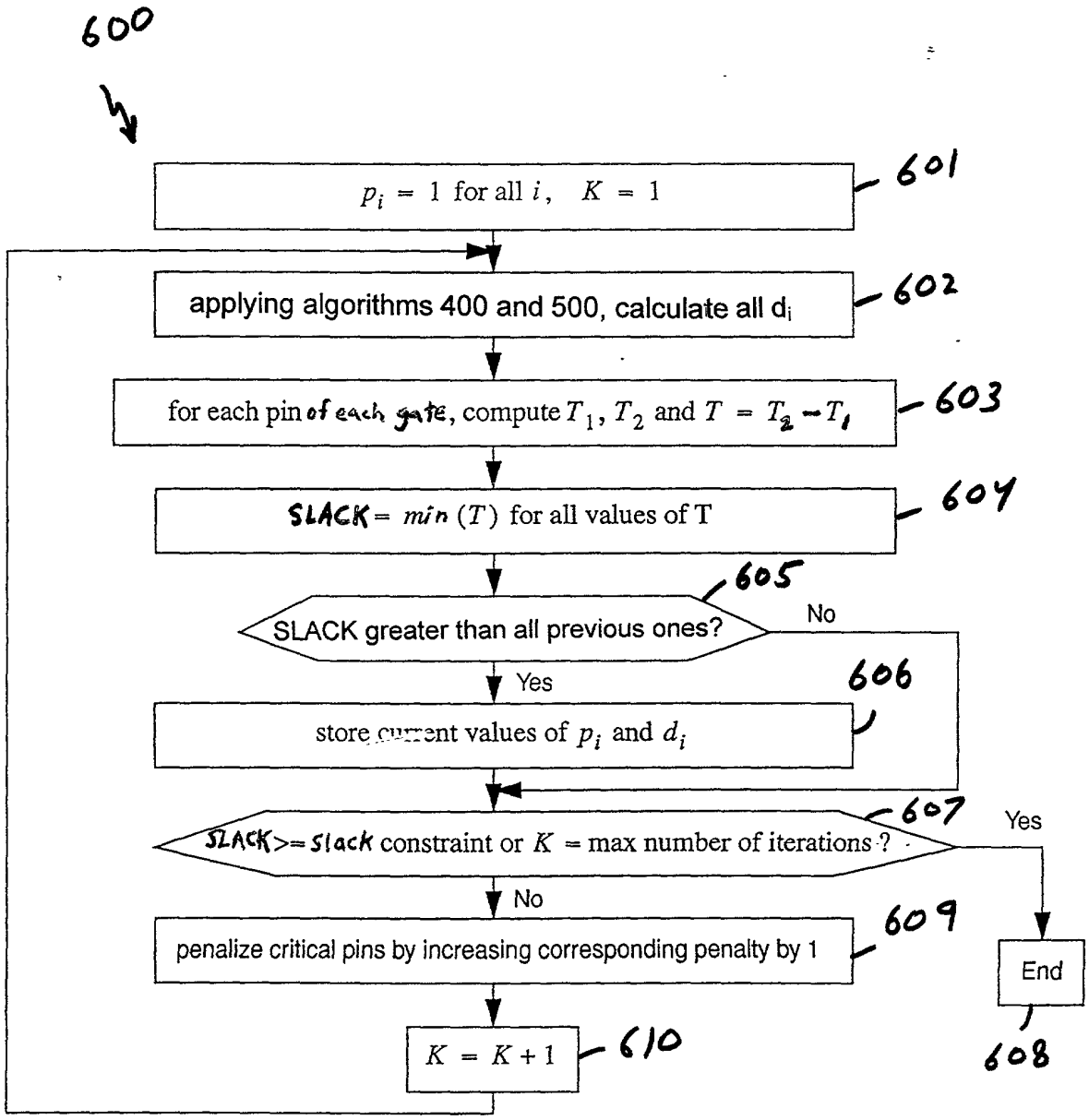
600
$p_i = 1$ for all i, $K = 1$
601
applying algorithms 400 and 500, calculate all d_i
602
for each pin of each gate, compute T_1, T_2 and $T = T_2 - T_1$
603
SLACK = min (T) for all values of T
604
SLACK greater than all previous ones?
605
No
Yes
store current values of p_i and d_i
606
SLACK>=slack constraint or K = max number of iterations ?
607
Yes
No
penalize critical pins by increasing corresponding penalty by 1
609
$K = K + 1$
610
End
608

FIG. 6

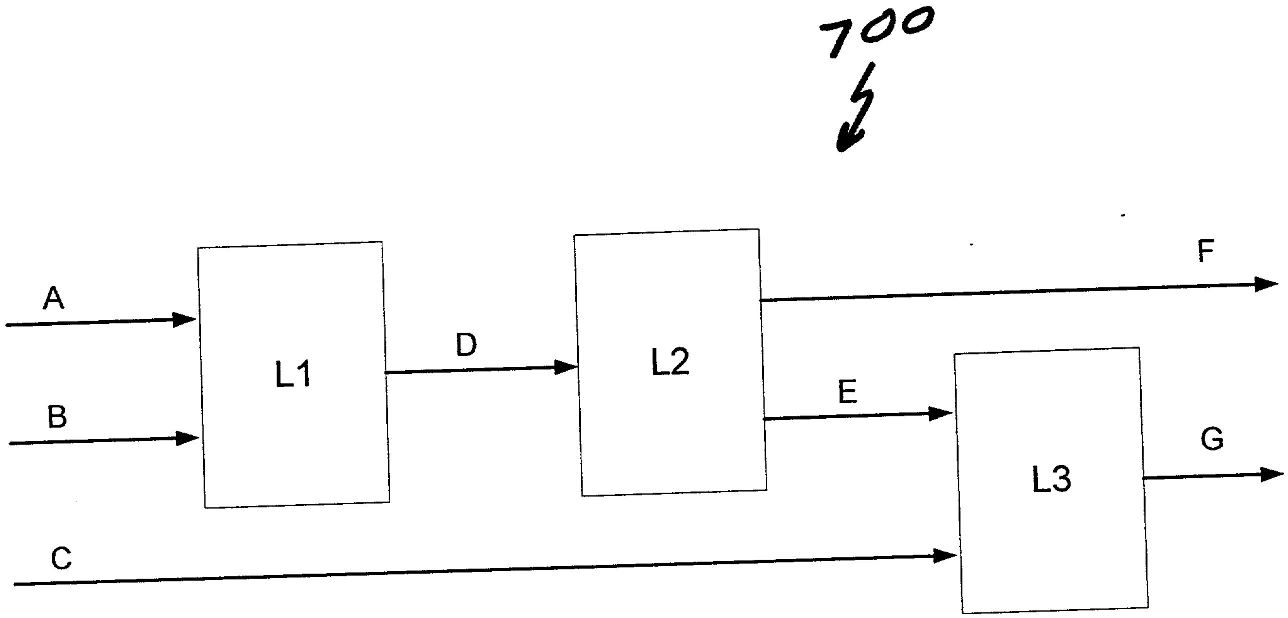

FIG. 7